

REMARKS

Favorable consideration of this application is respectfully requested.

Claims 1-28 are currently active in this case. Claim 4 has been amended, and Claims 29-40 have been added by way of the present amendment. Each new and amended claim is supported by the specification and claims as originally submitted and no new matter has been added.

In the outstanding Office Action Claim 4 was rejected under 35 U.S.C. §112 as being indefinite; Claims 1-3, 6-11 and 12-25 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Pauna* (U.S. Pat. No. 6,052,524) in view of *Testa et al.* (U.S. Pat. No. 6,205,407); and Claims 5, 11, 27 and 28 were rejected under 35 USC 103(a) as being unpatentable over *Pauna* in view of *Testa* and in further view of *Hill et al.* (U.S. Pat No. 6,438,415).

Applicants respectfully traverse the rejection of Claim 4 as being indefinite. However, Claim 4 has been amended in a manner that it is believed to render any such rejection moot. Accordingly, Applicants respectfully request that the rejection of Claim 4 under 35 USC 112, second paragraph, be withdrawn.

Applicants respectfully traverse the rejection of Claim 1 under 35 USC 103(a) as being obvious over *Pauna* and *Testa*. Claim 1 recites:

1. A method of modeling an electronic system
having both hardware and software elements,
comprising:
 capturing a plurality of behaviors that
correspond to operations performed by the system
being modeled;

capturing a plurality of hardware and software architectural components the plurality being contained within an architectural platform;

mapping each of the captured behaviors of the plurality of behaviors to a selected architectural component to perform the behavior;

recognizing and capturing communication patterns among the architectural components that require communication among them in order to perform the behaviors; and

mapping each instance of communication between behaviors to an instance of the captured pattern.

However, *Pauna* and *Testa* fail to teach or suggest similar subject matter.

Applicants respectfully traverse the assertion in the outstanding Office Action that states *"determination of timing and behavior violations is functionally equivalent to capturing a plurality of behaviors."* As a preliminary matter, Applicants respectfully note that in the context of *Pauna*, the determination of timing and behavior violations is an end result of the invention discussed in *Pauna* (see col. 5, lines 35-37 *"a method for determining timing and behavior violations for simulated hardware and software components is provided ..."*). However, Applicants claimed capturing of behaviors is a first step in implementing a modeling method. Accordingly, *Pauna's* determining of timing and behavior violations is entirely different from Applicants capture of behaviors.

Applicants also respectfully traverse the assertion that states *Pauna* teach *"mapping each of the captured behaviors of the plurality of behaviors to a selected architectural component to perform the behavior."* Referring first to the directly preceeding assertion, Applicants respectfully note that none of *Pauna's* timing and/or behavior violations are mapped. More importantly, Applicants respectfully note that the examples provided by *Pauna* at col. 8, lines 26-45 relate to the setting low level non-architectural parameters (e.g., setting clock speeds,), or items

for debugging (e.g., notifications of register changes), etc, for *Pauna*'s cycle accurate simulator. Therefore, the described interface is used to set up the simulator with correct clock speeds and other parameters, but does not provide mapping of captured behaviors to architectural components.

Accordingly, Applicants respectfully submit that Claim 1 is patentable over the combination of *Pauna* and *Testa* because the combined reference fail to teach or suggest subject matter specifically claimed in Claim 1.

Applicants respectfully traverse the rejection of Claim 27 under 35 USC 103(a) as being obvious over *Pauna* in view of *Testa*, and in view of *Hill*. Claim 27 recites:

27. A performance level model of the communications between behaviors of an electronic system having hardware and software components, the model comprising:

an application programming interface for a first behavior that provides data to be transferred to one or more destination behaviors;

a first service that implements the application programming interface that models the performance of the communication protocol, the first service being among a plurality of services supported by the pattern to which the behavior communication is mapped;

one or more application programming interfaces used by the first service to model performance of the architecture platform, the application interfaces being among a plurality of service declarations supported by the symbol of the architectural component to which the first behavior is mapped;

a supported service declaration on the symbol of the architecture component by a service definition, the service definition being among a plurality of service definitions specified by the performance model of the architecture component;

a second application interface that represents a function to be performed by a second architectural component topologically connected to the first component of the electronic system, the second service being one a plurality of second services each corresponding to a function capable of being performed by the second architectural component;

an input application interface on the destination behavior that receives output information of the performance level model of the electronic system, thereby completing a communication from source behavior to destination behavior.

However, the combined references of *Pauna*, *Testa*, and *Hill* fail to teach or suggest similar subject matter. In particular, Applicants respectfully note the above discussion related to *pauna*, and specifically that which relates to *Pauna's* interface to the cycle accurate simulator, which cannot be properly equated to Applicants claimed mapping of captured behaviors to selected architectural components for at least two reasons: 1. Because *Pauna's* interface sets low level details rather than architectural components; 2. Because *Pauna's* interface is not related to captured behaviors.

Therefore, even if *Pauna*, *Testa*, and *Hill* are combined, Applicants' claimed invention does not result. Accordingly, Applicants respectfully submit that Claim 27 is also patentable over the cited references. Based on the patentability of independent Claims 1 and 27, Applicants further respectfully submit that dependent Claims 2-26, and 28-40 are also patentable.

Applicants respectfully submit new Claims 29-40, each of which contain further patentably distinguishing details over the cited references. In particular, Applicants respectfully note new Claims 35, and 38-40 which include claimed subject matter related to mapping instances of communication to semaphore patterns that include sender/receiver pairs, and details related to categorization and selection of the pairs. However, the cited references provide no similar teachings. Accordingly, Applicants respectfully submit that new Claims 29-40 are also patentable.

Consequently, no further issues are believed to be outstanding, and it is respectfully submitted that this case is in condition for allowance. An early and favorable action is respectfully requested.

Dated: December 21, 2004

Respectfully submitted,

REED SMITH LLP

Two Embarcadero Center, Suite 2000
P.O. Box 7936
San Francisco, CA 94120-7936
Direct Dial: (415) 659-5927
Facsimile: (415) 391-8269

By: 

Name: John W. Carpenter

Reg. No. 39,129

DOCSSFO-12387490.1-JCARPENTER